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Remarks

Applicants respectfully request that this Amendment After Final Action be admitted under 37 C.F.R. § 1.116.

Applicants submit that this Amendment presents claims in better form for consideration on appeal. Furthermore, applicant believes that consideration of this Amendment could lead to favorable action that would remove one or more issues for appeal.

Claims 1, 15, 24 and 31 have been amended. No claims have been canceled. Therefore, claims 1-33 are now presented for examination.

Claims 1-3, 8, 10, 14-17, 21, 23-25, and 31-33 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shimoi et al. (U.S. Patent No. 5,652,857) and Corcoran et al. (U.S. Patent No. 6,449,689). Applicants submit that the present claims are patentable over any combination of Shimoi in view of Corcoran.

Shimoi discloses a disk control apparatus for recording and reproducing compression data to physical device of direct access type. The apparatus includes a cache memory between a host computer and a disk drive. The cache memory is divided into a non-compression cache memory for storing non-compression data on a logic block unit basis and a compression cache memory for storing compression data on a compression group unit basis having the same size as that of the logic sector of the disk drive. A compressing circuit extracts the data stored in the non-compression cache memory on a logic block unit basis and compresses the data. A compression group forming unit collects the compression data of the logic block unit by the compressing circuit unit, thereby forming a compression group and storing the compression group into the compression cache memory. An expanding circuit unit extracts the data stored in the

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compression cache memory on a compression group unit basis, expands, and develops into the non-compression cache memory. See Shimoi at col. 3, ll. 23-65.

Corcoran discloses a system and method for organizing compressed data on a storage disk to increase storage density. The method and system include a compressor for compressing a data block into a compressed data block, wherein N represents a compression ratio. The storage disk includes a first storage partition having N slots for storing compressed data, and a second storage partition also having N slots for storing overflow data. Each of the N slots in the first partition includes at least one address pointer for pointing to locations in the second partition. According to a further aspect of the system and method, if the compressed data block is less than or equal to $1/N$ of the data block size, then the compressed data block is stored in a first slot in the first storage partition. If the compressed data block is greater than $1/N$ of the data block size, then the first $1/N$ of the compressed data block is stored in the first slot in the first storage partition and a remainder of the compressed block is stored in one or more slots in the second storage partition. The address pointer in the first slot is then updated to point to the one or more slots in the second storage partition. See Corcoran at Abstract.

Claim 1 of the present application recites:

A computer system comprising:
a central processing unit (CPU); and
a cache memory, coupled to the CPU, including:
a main cache having a plurality of cache lines, each
of the plurality of cache lines being compressible to
form compressed cache lines to store additional data;
and
a plurality of storage pools to hold a segment of the
additional data for a compressed cache line; and
a cache controller having compression logic to
determine that a cache line retrieved from a main
memory device is to be combined with a resident

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companion cache line to form the compressed cache line if the companion cache line is resident in the cache memory and to store the compressed cache line in the cache line of the resident companion.

Applicants submit that neither Shimoi nor disclose or suggest determining that a cache line retrieved from a main memory device is to be combined with a resident companion cache line to form a compressed cache line if the companion cache line is resident in the cache memory.

The Final Office Action asserts that Shimoi at column 10, line 10 – column 11, line 12 discloses that cache lines are retrieved from the cache memory and combined together to form a compression group. See Final Office Action at page 16, paragraph 31. Nevertheless, there is no disclosure, or reasonable suggestion in Shimoi of a process of *determining that a cache line retrieved from a main memory device is to be combined with a resident companion cache line to form a compressed cache line if the companion cache line is resident in the cache memory.*

Because, Shimoi and Corcoran both fail to disclose or suggest determining that a cache line retrieved from a main memory device is to be combined with a resident companion cache line to form a compressed cache line if the companion cache line is resident in the cache memory, any combination of Shimoi and Corcoran would also fail to disclose or suggest such features. Therefore claim 1, and its dependent claims, is patentable over the combination of Shimoi and Corcoran since.

Independent claims 15, 24 and 31 include limitations similar to those recited in claim 1. Thus, claims 15, 24 and 31, and their respective dependent claims, are patentable over the combination of Shimoi and Corcoran for the reasons stated above with respect to claim 1.

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Claims 4-7, 9, 18-20, 22, and 26-30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shimoi and Corcoran further in view of Obara (U.S. Patent No. 6,115,787). Applicants submit that the present claims are patentable over any combination of Shimoi in view of Corcoran even in view of Obara.

Obara discloses storing compressed records into a cache memory of a disk storage system in an easy-to-read manner. Data to be stored in the cache memory is divided into plural data blocks each having two cache blocks in association with track blocks to which the data belongs and are compressed. The respective data blocks after the compression are stored in one or plural cache blocks. Information for retrieving each cache block from an in-track address for the data block is stored as part of retrieval information for the cache memory. When the respective data blocks in a record is read, the cache block storing the compressed data block is determined based on the in-track address of the data block and the retrieval information. See Obara at Abstract.

However, Obara does not disclose or suggest determining that a cache line retrieved from a main memory device is to be combined with a resident companion cache line to form a compressed cache line if the companion cache line is resident in the cache memory. As discussed above, Shimoi and Corcoran all fail to disclose or suggest such features. Therefore, any combination of Shimoi, Corcoran and Obara would also not disclose or suggest the features. As a result, the present claims are patentable over the combination of Shimoi, Corcoran and Obara.

Claims 11-13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shimoi, Corcoran and further in view of Cypher (U.S. Patent No. 6,629,205). Applicants

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submit that the present claims are patentable over any combination of Shimoi, Corcoran, and Cypher.

Cypher discloses a cache memory including a plurality of memory chips that are configured to collectively store a plurality of cache lines. Each cache line includes data and an associated cache tag. The cache tag may include an address tag which identifies the line as well as state information indicating the coherency state for the line. Each cache line is stored across the memory chips in a row formed by corresponding entries (i.e., entries accessed using the same index address). The plurality of cache lines is grouped into separate subsets based on index addresses, thereby forming several separate classes of cache lines. The cache tags associated with cache lines of different classes are stored in different memory chips. During operation, the cache controller may receive multiple snoop requests corresponding to, for example, transactions initiated by various processors. The cache controller is configured to concurrently access the cache tags of multiple lines in response to the snoop requests if the lines correspond to differing classes. See Cypher at Abstract.

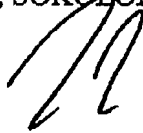
Nonetheless, Cypher does not disclose or suggest determining that a cache line retrieved from a main memory device is to be combined with a resident companion cache line to form a compressed cache line if the companion cache line is resident in the cache memory. As discussed above, Shimoi and Corcoran fail to disclose or suggest such limitations. Therefore, any combination of Shimoi, Corcoran and Cypher would also not disclose or suggest the limitations. Accordingly, the present claims are patentable over the combination of Shimoi, Corcoran, and Cypher.

Applicants submit that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
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Date: August 2, 2007

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